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EXAMINER	
LOUIE, OSCAR A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,818	BUSSON ET AL.	
	Examiner	Art Unit	
	OSCAR A. LOUIE	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/08/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This final action is in response to the amendment filed on 01/03/2008. In light of the applicant's amendments, the examiner hereby withdraws his previous 35 U.S.C. 112 2nd paragraph rejections regarding Claims 1, 2, 4, 10, & 21. Claims 1-55 are pending and have been considered as follows.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 & 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomasz et al. (US-6031878-A).

Claim 1:

Tomasz et al. disclose an electronic component comprising,

- "an integrated circuit embodied on a monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];

- "a tuning module of the direct sampling type that is able to receive satellite digital television analog signals composed of several channels" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8];
- "several channel decoding digital modules connected at an output of the tuning module so as to deliver respectively simultaneously several streams of data packets corresponding to several different selected channels" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27].

Claim 9:

Tomasz et al. disclose an electronic component, as in Claim 1 above, further comprising,

- "the electronic component comprises a satellite digital television signal receiver" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 10, 11, 13-15, 20, 38, 48-50, & 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A).

Claim 2:

Tomasz et al. disclose an electronic component, as in Claim 1 above, further comprising,

- "the channels extend over a predetermined frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];
- "the analog signals convey digital information coded by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61];
- "the tuning module comprises: an analog stage receiving the said analog signals" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable") [column 3 lines 5-6];
- "the tuning module comprises: a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the said frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as

high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52];

but, Tomasz et al. do not disclose,

- "the tuning module comprises: several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and are able to deliver simultaneously respectively several sampled digital signals centered around the zero frequency and corresponding respectively to several selected channels"

however, Robbins et al. do disclose,

- "This signal is input both to a mixer and Nyquist filter block 72 and the carrier recovery block 74. In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82. The recovered carrier is first passed through a Nyquist delay 84 which compensates for the delay of the Nyquist filter 80. The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization" [column 7 lines 8-17];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the tuning module comprises: several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and are

able to deliver simultaneously respectively several sampled digital signals centered around the zero frequency and corresponding respectively to several selected channels," in the invention as disclosed by Tomasz et al. for the purposes of providing additional channel filtering.

Claim 10:

Tomasz et al. disclose an integrated circuit comprising,

- "a monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];
- "an input receiving an analog signal including a plurality of channels" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8];
- "a first channel decoding digital module connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

- "a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

but, Tomasz et al. do not disclose,

- "an analog-to-digital converter to convert the analog signal to a digital signal"
- "a first digital tuner that downconverts the digital signal to a first downconverted digital signal"
- "information of a selected first channel in the downconverted digital signal is centered at around zero frequency"
- "a second digital tuner that downconverts the digital signal to a second downconverted digital signal"
- "information of a selected second channel in the downconverted digital signal is centered at around zero frequency"

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24" [column 5 lines 1-3];

- "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82" [column 7 lines 9-12];
- "The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization. For NTSC signals, the double sideband component is from 0-0.75 MHz and-the single sideband component is from 0.75-4.2 MHz" [column 7 lines 14-19];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "an analog-to-digital converter to convert the analog signal to a digital signal" and "a first digital tuner that downconverts the digital signal to a first downconverted digital signal" and "information of a selected first channel in the downconverted digital signal is centered at around zero frequency" and "a second digital tuner that downconverts the digital signal to a second downconverted digital signal" and "information of a selected second channel in the downconverted digital signal is centered at around zero frequency," in the invention as disclosed by Tomasz et al. for the purposes of timing and data recovery and providing additional adjacent channel filtering. In addition, it is understood that a plurality of decoders and tuners may be present in the system to handle multiple simultaneous signals.

Claim 11:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further comprising,

- "the first and second digital tuners are each of a direct sampling type which performs frequency transposition and channel selection in a digital domain" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8].

Claim 13:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further comprising,

- "the analog signal conveys information for the plurality of channels by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 14:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further comprising,

- "the channels of the analog signal extend over a frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

- "the analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52].

Claim 15:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 14 above, further comprising,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 20:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further comprising,

- "the integrated circuit is a component within a satellite digital television signal receiver" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 38:

Tomasz et al. disclose an electronic device comprising,

- "an integrated circuit embodied on a monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];
- "a multi-channel direct sampling type tuner that receives an analog signal composed of several channels and outputs first and second channel digital signals" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8];

but, Tomasz et al. do not disclose,

- "a first channel decoder that receives the first channel digital signal and outputs a first channel stream of data packets"

- "a second channel decoder that receives the second channel digital signal and outputs a second channel stream of data packets"

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24" [column 5 lines 1-3];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a first channel decoder that receives the first channel digital signal and outputs a first channel stream of data packets" and "a second channel decoder that receives the second channel digital signal and outputs a second channel stream of data packets," in the invention as disclosed by Tomasz et al. for the purposes of timing and data recovery.

Claim 48:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further comprising,

- "the analog signal conveys information for the plurality of channels by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 49:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further comprising,

- "the channels of the analog signal extend over a frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];
- "the analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52].

Claim 50:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 49 above, further comprising,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 55:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further comprising,

- "the integrated circuit is a component within a satellite digital television signal receiver" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

5. Claims 7 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Lieber et al. (US-5220164-A).

Claim 7:

Tomasz et al. disclose an electronic component, as in Claim 1 above, but do not disclose,

- "a grounding metal plate glued to a rear face of the substrate by a conducting glue"

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer" [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a grounding metal plate glued to a rear face of the substrate by a conducting glue," in the invention as disclosed by Tomasz et al. for the purposes of providing both imaging and ranging functions.

Claim 8:

Tomasz et al. disclose an electronic component, as in Claim 1 above, but do not disclose,

- "the substrate has a first type of conductivity"
- "elements performing a digital processing are disposed in a part of the substrate that is insulated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity"
- "the semiconducting barrier is biased by a bias voltage different from that used for the insulated part of the substrate"

however, Lieber et al. do disclose,

- "The detection of the prompt electrical current is made through a transformer that couples the anode to a power supply" [column 3 lines 41-43];
- "The power supply biases the anode relative to the MCP and photocathode such that the MCP is grounded, with the anode being biased positively relative to the MCP, and the photocathode being biased negatively relative to the MCP" [column 3 lines 44-48];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the substrate has a first type of conductivity" and "elements performing a digital processing are disposed in a part of the substrate that is insulated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity" and "the semiconducting barrier is biased by a bias voltage different from that used for the insulated part of the substrate," in the invention as

disclosed by Tomasz et al. for the purposes of allowing the prompt anode current to be detected without having to ground the anode and the use of a non-grounded anode significantly simplifies the power supply circuitry.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Hwang et al. (US-4894657-A).

Claim 3:

Tomasz et al. disclose an electronic component, as in Claim 1 above, further comprising,

- "the channels extend over a predetermined frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];
- "the analog signals convey digital information coded by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61];
- "each channel decoding module comprises: a decimator filter followed by an additional digital filter for eliminating information of adjacent channels" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but they do not disclose,

- "each channel decoding module comprises: an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel being processed by the channel decoding module"

however, Hwang et al. do disclose,

- "The calibrator is employed due to the need for calibration (or digital correction) arising out of the nonlinearity that may be present in pipelined A/D converters with greater than 8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "each channel decoding module comprises: an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel being processed by the channel decoding module," in the invention as disclosed by Tomasz et al. for the purposes of digital correction.

7. Claims 4-6, 16-18, & 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Hwang et al. (US-4894657-A).

Claim 4:

Tomasz et al. disclose an electronic component, as in Claim 1 above, further comprising,

- "the channels extend over a predetermined frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];

- "the analog signals convey digital information coded by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61];
- "the tuning module comprises: an analog stage receiving the said analog signals" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable") [column 3 lines 5-6];
- "the tuning module comprises: a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the said frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52];
- "each channel decoding module comprises: a decimator filter followed by an additional digital filter for eliminating information of adjacent channels" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal

oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but, they do not disclose,

- "the tuning module comprises: several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and are able to deliver simultaneously respectively several sampled digital signals centered around the zero frequency and corresponding respectively to several selected channels"
- "each channel decoding module comprises: an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding module"

however, Robbins et al. do disclose,

- "This signal is input both to a mixer and Nyquist filter block 72 and the carrier recovery block 74. In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82. The recovered carrier is first passed through a Nyquist delay 84 which compensates for the delay of the Nyquist filter 80. The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization" [column 7 lines 8-17]];

and the combination of Tomasz et al. and Robbins et al. do not disclose,

- "each channel decoding module comprises: an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding module"

where as, Hwang et al. do disclose,

- "The calibrator is employed due to the need for calibration (or digital correction) arising out of the nonlinearity that may be present in pipelined A/D converters with greater than 8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the tuning module comprises: several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and are able to deliver simultaneously respectively several sampled digital signals centered around the zero frequency and corresponding respectively to several selected channels" and "each channel decoding module comprises: an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding module," in the invention as disclosed by Tomasz et al. for the purposes of channel filtering and digital correction.

Claim 5:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic component, as in Claim 4 above, but their combination do not disclose,

- "the resolution of the analog/digital conversion stage is greater than or equal to 6 bits"

however, Hwang et al. do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A converter 16 may be of the capacitive type, which is capable of converting as many as ten bits without being unduly tolerance-dependent" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the resolution of the analog/digital conversion stage is greater than or equal to 6 bits," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of achieving accurate resolution of the output and without being tolerance dependent.

Claim 6:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic component, as in Claim 4 above, but their combination do not disclose,

- "the decimator filter is a low-pass filter whose cutoff frequency is of the order of twice the frequency half-width of a channel"
- "the cutoff frequency of the additional digital filter is of the order of the frequency half-width of a channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the decimator filter is a low-pass filter whose cutoff frequency is of the order of twice the frequency half-width of a channel" and "the cutoff frequency of the additional digital filter is of the order of the frequency half-width of a channel," in the invention as disclosed by Tomasz et al. and Hwang et al. for the purposes of providing additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization.

Claim 16:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, further comprising,

- "a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

- "a digital filter that filters out the adjacent channel information" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44].

but they do not disclose,

- "an error correction stage to produce the data packets from the selected channel information"

however, Hwang et al. do disclose,

- "The calibrator is employed due to the need for calibration (or digital correction) arising out of the nonlinearity that may be present in pipelined A/D converters with greater than 8- or 9-bit resolution" [column 3 lines 26-30];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "an error correction stage to produce the data packets from the selected channel information," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of digital correction.

Claim 17:

Tomasz et al., Robbins et al., and Hwang et al. disclose an integrated circuit, as in Claim 16 above, but their combination do not disclose,

- "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel," in the invention as disclosed by Tomasz et al. and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

Claim 18:

Tomasz et al., Robbins et al., and Hwang et al. disclose an integrated circuit, as in Claim 17 above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel," in the invention as disclosed by Tomasz et al. and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

Claim 51:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, further comprising,

- "a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

- "a digital filter that filters out the adjacent channel information" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but their combination do not disclose,

- "an error correction stage to produce the data packets from the selected channel information"

however, Hwang et al. do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A converter 16 may be of the capacitive type, which is capable of converting as many as ten bits without being unduly tolerance-dependent"" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "an error correction stage to produce the data packets from the selected channel information," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of converting as many as ten bits without being unduly tolerance-dependent.

Claim 52:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic device, as in Claim 51 above, but their combination do not disclose,

- "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel," in the invention as disclosed by Tomasz et al., Robbins et al., and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

Claim 53:

Tomasz et al., Robbins et al., and Hwang et al. disclose an electronic device, as in Claim 52 above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel"
- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel," in the invention as disclosed by Tomasz et al., Robbins et al., and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

8. Claims 21-28, 30-32, 37, 39, & 40-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young (EP-0481543-A1).

Claim 21:

Tomasz et al. disclose an integrated circuit comprising,

- "a monolithic substrate" (i.e. "the preferred embodiment by a single integrated circuit, so as to eliminate many components required or at least used in prior art systems to obtain and process the signal") [column 2 lines 59-62];
- "an input receiving an analog signal including a plurality of channels" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8];

- "a first channel decoding digital module connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];
- "a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel" (i.e. "The integrated circuit includes a variable gain amplifier 66, which amplifier will be more fully described in detail later herein, which provides a wide range of automatic gain control and high linearity to provide acceptably low cross-talk between channels in the output thereof. The output of the amplifier 66 of course is a broadband output, containing in the preferred embodiment, all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 19-27];

but they do not disclose,

- "a first analog-to-digital converter to convert the analog signal to a first digital signal"
- "a second analog-to-digital converter to convert the analog signal to a second digital signal"
- "a first digital tuner that downconverts a received digital signal to a first downconverted digital signal"

- "information of a selected first channel in the downconverted digital signal is centered at around zero frequency"
- "a second digital tuner that downconverts a received digital signal to a second downconverted digital signal"
- "information of a selected second channel in the downconverted digital signal is centered at around zero frequency"
- "a switching circuit that selectively couples the first and second digital signals to the first and second digital tuners"

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24" [column 5 lines 1-3];
- "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82" [column 7 lines 9-12];
- "The Nyquist filter is a lowpass filter that provides additional adjacent channel filtering as well as VSB double-single sideband magnitude equalization. For NTSC signals, the double sideband component is from 0-0.75 MHz and-the single sideband component is from 0.75-4.2 MHz" [column 7 lines 14-19];

and the combination of Tomasz et al. and Robbins et al. do not disclose,

- "a switching circuit that selectively couples the first and second digital signals to the first and second digital tuners"

where as, Young does disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a first analog-to-digital converter to convert the analog signal to a first digital signal" and "a second analog-to-digital converter to convert the analog signal to a second digital signal" and "a first digital tuner that downconverts a received digital signal to a first downconverted digital signal" and "information of a selected first channel in the downconverted digital signal is centered at around zero frequency" and "a second digital tuner that downconverts a received digital signal to a second downconverted digital signal" and "information of a selected second channel in the downconverted digital signal is centered at around zero frequency" and "a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel" and "a switching circuit that selectively couples the first and second digital signals to the first and second digital tuners," in the invention as disclosed by Tomasz et al. for the purposes of having the outputs either all connected to their first respective inputs or to their second respective inputs simultaneously.

Claim 22:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, but their combination do not disclose,

- "the first analog-to-digital converter is associated with analog signals in a first passband"
- "the second analog-to-digital converter is associated with analog signals in a second passband"

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24. The video DSP demodulates and unscrambles video from an intermediate frequency (IF) carrier. The carrier can comprise, for example, a low IF frequency carrier such as a carrier centered at 9 MHz plus or minus 100 KHz. The video DSP consists of an analog-to-digital (A/D) converter 14, video demodulator 16, and a video descrambler 18" [column 5 lines 1-8];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the first analog-to-digital converter is associated with analog signals in a first passband" and "the second analog-to-digital converter is associated with analog signals in a second passband," in the invention as disclosed by Tomasz et al. and Young since it is understood that there may be a plurality of analog to digital converters where each converter would correspond with its own input.

Claims 23-27:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 22 above, but their combination do not disclose,

- "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital tuners to the first analog-to-digital converter"
- "if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second digital tuners to the second analog-to-digital converter"
- "if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first digital tuner to the first analog-to-digital converter and the second digital tuner to the second analog-to-digital converter"
- "if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first digital tuner to the second analog-to-digital converter and the second digital tuner to the first analog-to-digital converter"
- "a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter"
- "a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter"

however, Young do disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital tuners to the first analog-to-digital converter," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of having their outputs either all connected to their first respective inputs or to their second respective inputs simultaneously.

Claim 28:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, further disclosing,

- "the first and second digital tuners are each of a direct sampling type which performs frequency transposition and channel selection in a digital domain" (i.e. "the tuner unit will have an input connector 56 for receiving the signal on cable 54, and an output connector 58 which may be used for coupling the received signal to a second set top box, if needed") [column 3 lines 5-8].

Claim 30:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, further disclosing,

- "the analog signal conveys information for the plurality of channels by digital modulation" (i.e. "Whether discrete filters or active filters are used, the output of the filters will be digitized by analog to digital converters 100 and then demodulated by the DSP for recovery of the digital data") [column 4 lines 58-61].

Claim 31:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, further disclosing,

- "the channels of the analog signal applied to each analog-to-digital converter extend over a given frequency span" (i.e. "all the channels in the 950 MHz to 2150 MHz DBS signal bandwidth") [column 3 lines 26-27];
- "each analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the given frequency span" (i.e. "The level of the local oscillator signal in the RF signal input to the mixers is approximately -50 dBm. The signal present may be as low as -70 dBm, so that if uncorrected, the DC offset may be as high as 20 dBm greater than the signal of interest. In order to avoid saturation of the amplifiers on the output of the mixers, feedback of the DC offset is provided from the amplifier chain to the output of the mixers, as shown in FIGS. 2 and 3. DC offset correction circuitry in general is well known, and need not be described in detail herein") [column 4 lines 43-52].

Claim 32:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 31 above, further disclosing,

- "the analog signal comprises a satellite digital television analog signal" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claim 37:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, further disclosing,

- "the integrated circuit is a component within a satellite digital television signal receiver" (i.e. "The direct broadcast satellite signal received from the satellite dish is amplified and then downshifted within the Low Noise Block (LNB), a subsystem contained with the satellite dish assembly, to a predetermined frequency band, typically in the L-band in the range 950 MHz to 2150 MHz") [column 2 lines 65-67 & column 3 lines 1-3].

Claims 39 & 40:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, Robbins et al. further disclosing,

- "at least one analog-to-digital converter to convert the received analog signal to a digital signal" (i.e. "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24") [column 5 lines 1-3];
- "a first frequency transposition circuit that downconverts the digital signal to the first channel digital signal" (i.e. "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82") [column 7 lines 9-12];
- "a second frequency transposition circuit that downconverts the digital signal to the second channel digital signal" (i.e. "In the mixer and Nyquist filter block 72, the video IF is first Nyquist filtered via Nyquist filter 80 and then downconverted to baseband by mixing it with the recovered carrier in mixer 82") [column 7 lines 9-12];
- "the multi-channel direct sampling type tuner comprises a first and second analog-to-digital converter that convert the received analog signal to a first and second digital signal" (i.e. "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24") [column 5 lines 1-3];

but their combination do not disclose,

- "the multi-channel direct sampling type tuner comprises a switching circuit that selectively couples the first and second digital signals to the first and second frequency transposition circuits"

however, Young does disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the multi-channel direct sampling type tuner comprises a switching circuit that selectively couples the first and second digital signals to the first and second frequency transposition circuits," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of having their outputs either all connected to their first respective inputs or to their second respective inputs simultaneously.

Claim 41:

Tomasz et al., Robbins et al., and Young disclose an electronic device, as in Claim 40 above, but their combination do not disclose,

- "the first analog-to-digital converter is associated with analog signals in a first passband"
- "the second analog-to-digital converter is associated with analog signals in a second passband"

however, Robbins et al. do disclose,

- "An overall block diagram of the television converter is illustrated in FIG. 1. The converter includes a video DSP 12, audio DSP 26, and timing and data recovery circuitry 24. The video DSP demodulates and unscrambles video from an intermediate frequency (IF) carrier. The carrier can comprise, for example, a low IF frequency carrier such as a carrier centered at 9 MHz plus or minus 100 KHz. The video DSP consists of an analog-to-digital (A/D) converter 14, video demodulator 16, and a video descrambler 18" [column 5 lines 1-8];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the first analog-to-digital converter is associated with analog signals in a first passband" and "the second analog-to-digital converter is associated with analog signals in a second passband," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of timing and data recovery.

Claims 42-46:

Tomasz et al., Robbins et al., and Young disclose an electronic device, as in Claim 41 above, but their combination do not disclose,

- "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second frequency transposition circuits to the first analog-to-digital converter"
- "if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second frequency transposition circuits to the second analog-to-digital converter"

- "if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first frequency transposition circuit to the first analog-to-digital converter and the second frequency transposition circuit to the second analog-to-digital converter"
- "if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first frequency transposition circuit to the second analog-to-digital converter and the second frequency transposition circuit to the first analog-to-digital converter"
- "a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter"
- "a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter"

however, Robbins et al. do disclose,

- "Each of the three switches 50a, 50b and 50c has a first input, a second input, and a moving contact which can connect an output to either of the inputs. The three switches are ganged together so that their outputs are either all connected to their first respective inputs or to their second respective inputs simultaneously" [column 3 lines 38-44];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second frequency transposition circuits to the first analog-to-digital converter" and "if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second frequency

transposition circuits to the second analog-to-digital converter" and "if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first frequency transposition circuit to the first analog-to-digital converter and the second frequency transposition circuit to the second analog-to-digital converter" and "if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first frequency transposition circuit to the second analog-to-digital converter and the second frequency transposition circuit to the first analog-to-digital converter," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of having their outputs either all connected to their first respective inputs or to their second respective inputs simultaneously.

9. Claims 12 & 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Dapper et al. (US-6275990-B1).

Claim 12:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, but they do not disclose,

- "the analog-to-digital converter oversamples the received analog signal"

however, Dapper et al. do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the analog-to-digital converter oversamples the received analog signal," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of achieving high resolution.

Claim 47:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, but they do not disclose,

- "the analog-to-digital converter oversamples the received analog signal"

however, Dapper et al. do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the analog-to-digital converter oversamples the received analog signal," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of achieving high resolution.

10. Claims 19 & 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Lieber et al. (US-5220164-A).

Claim 19:

Tomasz et al. and Robbins et al. disclose an integrated circuit, as in Claim 10 above, but they do not disclose,

- "a metal plate attached to a rear surface of the substrate"

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer" [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a metal plate attached to a rear surface of the substrate," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of allowing some of the electrons striking the anode to be detected as a prompt electrical current.

Claim 54:

Tomasz et al. and Robbins et al. disclose an electronic device, as in Claim 38 above, but they do not disclose,

- "a metal plate attached to a rear surface of the substrate"

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer" [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a metal plate attached to a rear surface of the substrate," in the invention as disclosed by Tomasz et al. and Robbins et al. for the purposes of allowing some of the electrons striking the anode to be detected as a prompt electrical current.

11. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young (EP-0481543-A1) and in further view of Dapper et al. (US-6275990-B1).

Claim 29:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, but they do not disclose,

- "each analog-to-digital converter oversamples the received analog signal"

however, Dapper et al. do disclose,

- "Sigma Delta converter 2840 achieves high resolution by oversampling the input signal at a frequency much above the Nyquist frequency" [column 94 lines 23-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "each analog-to-digital converter oversamples the received analog signal," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of achieving high resolution.

12. Claim 33-35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young (EP-0481543-A1) and in further view of Hwang et al. (US-4894657-A).

Claim 33:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, further disclosing,

- "a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information" (i.e. "the output of the

VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

- "a digital filter that filters out the adjacent channel information" (i.e. "the output of the VCO is fed back, divided down by the ratio of the expected carrier frequency of the desired channel to the frequency of the crystal oscillator and then compared to the crystal oscillator frequency. The deviation in the external voltage controlled oscillator frequency is used to control the tank circuit to readjust the output frequency of the voltage controlled oscillator") [column 3 lines 38-44];

but they do not disclose,

- "an error correction stage to produce the data packets from the selected channel information"

however, Hwang et al. do disclose,

- "accurate resolution of the output code from flash A/D subconverter 10 is desired, D/A converter 16 may be of the capacitive type, which is capable of converting as many as ten bits without being unduly tolerance-dependent" [column 3 lines 9-10];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "an error correction stage to produce the data packets from the selected channel information," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of converting as many as ten bits without being unduly tolerance-dependent.

Claim 34:

Tomasz et al., Robbins et al., Young, and Hwang et al. disclose an integrated circuit, as in Claim 33 above, but their combination do not disclose,

- "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel," in the invention as disclosed by Tomasz et al., Young, and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

Claim 35:

Tomasz et al., Robbins et al., Young, and Hwang et al. disclose an integrated circuit, as in Claim 34 above, but their combination do not disclose,

- "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel"

however, Robbins et al. do disclose,

- "The Nyquist filter 80 can be implemented as a finite impulse response (FIR) lowpass filter having, for example, a sampling frequency of 27 MHz, passband edge of 7.75 MHz, passband attenuation of 0.5 dB, stopband edge of 10.25 MHz, stopband attenuation of 40 dB, beta of 3.3953 and -6 dB cutoff frequency of 9 MHz" [column 7 lines 20-26];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel," in the invention as disclosed by Tomasz et al., Young, and Hwang et al. for the purposes of implementing a Nyquist filter as a finite impulse response (FIR) lowpass filter.

13. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (US-6031878-A) in view of Robbins et al. (US-6147713-A) and in further view of Young (EP-0481543-A1) and in further view of Lieber et al. (US-5220164-A).

Claim 36:

Tomasz et al., Robbins et al., and Young disclose an integrated circuit, as in Claim 21 above, but they do not disclose,

- "a metal plate attached to a rear surface of the substrate"

however, Lieber et al. do disclose,

- "The single detection element includes an opaque photocathode, a microchannel plate (MCP) electron multiplier, and a phosphor coated anode covered with a metalized layer" [column 3 lines 36-39];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a metal plate attached to a rear surface of the substrate," in the invention as disclosed by Tomasz et al., Robbins et al., and Young for the purposes of allowing some of the electrons striking the anode to be detected as a prompt electrical current.

Response to Arguments

14. Applicant's arguments filed 12/28/2008 have been fully considered but they are not persuasive.

- Applicant's argument regarding independent Claims 1, 10, 21, & 38 and their dependents stating that the prior art of record individually or in any combination do not disclose all of the integrated circuit limitations as part of the same monolithic substrate, has been considered but is non-persuasive. The examiner notes that by definition of an "integrated circuit" each integrated circuit is implied as having to be part of the same substrate in order for them to be interconnected to one another as one functioning integrated circuit made up of individual modules of integrated circuits.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
03/17/2008

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136